Fault

Open Source EDA's Missing DFT Toolchain

https://github.com/Cloud-V/Fault

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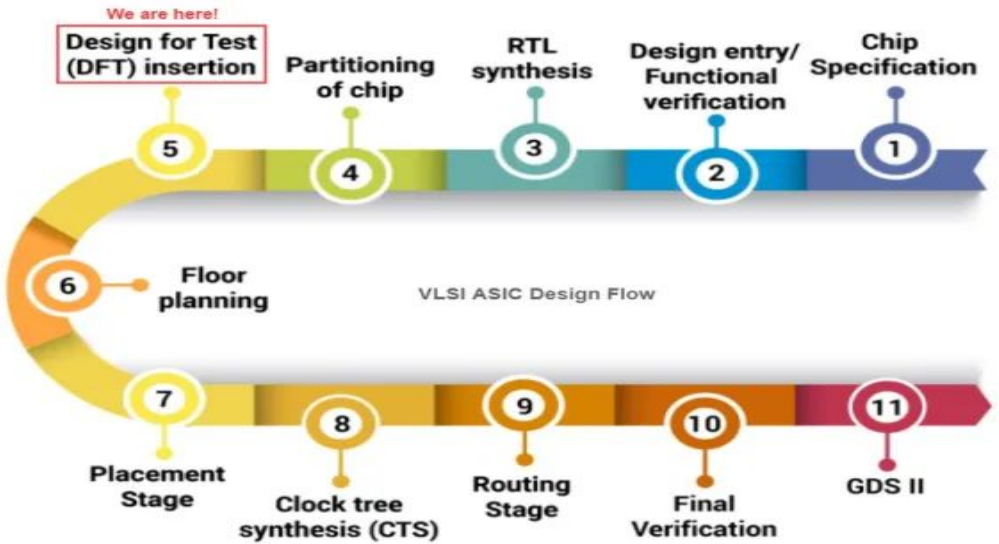
AUC

What is DFT (Design–For–Testing) ?

➔ Design for testing/DFT is mainly concerned with inserting extra-logic into the design to make it testable after manufacturing.



Source: https://technobyte.org/what-is-dft-design-for-testability-introduction/

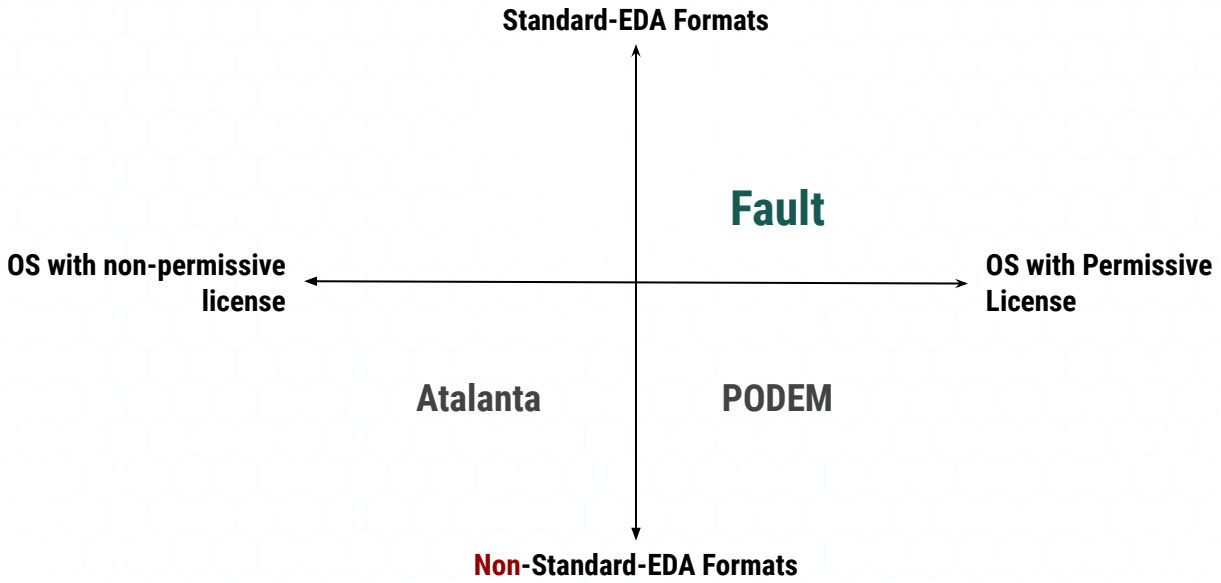
Why DFT ?

“ The Rule of 10”

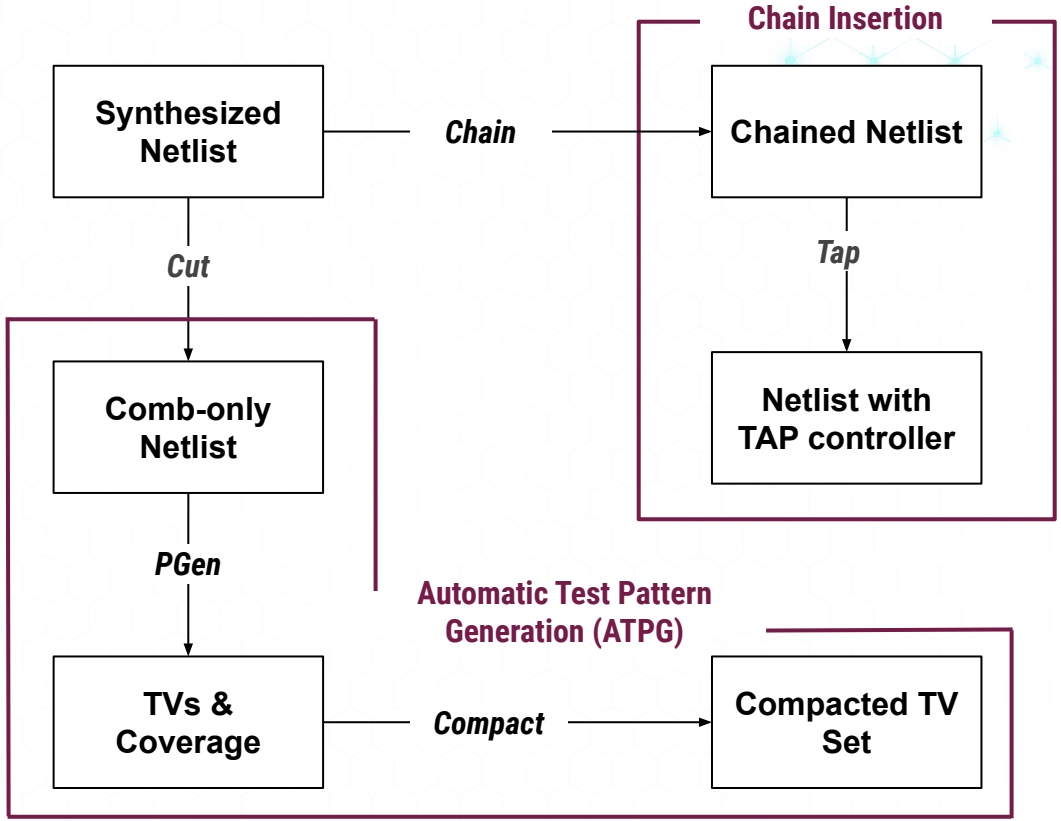
➔ Failure to detect a faulty chip incurs a cost that continues to get multiplied by 10 as the chip goes from packaging till the end user.

Why Fault ?

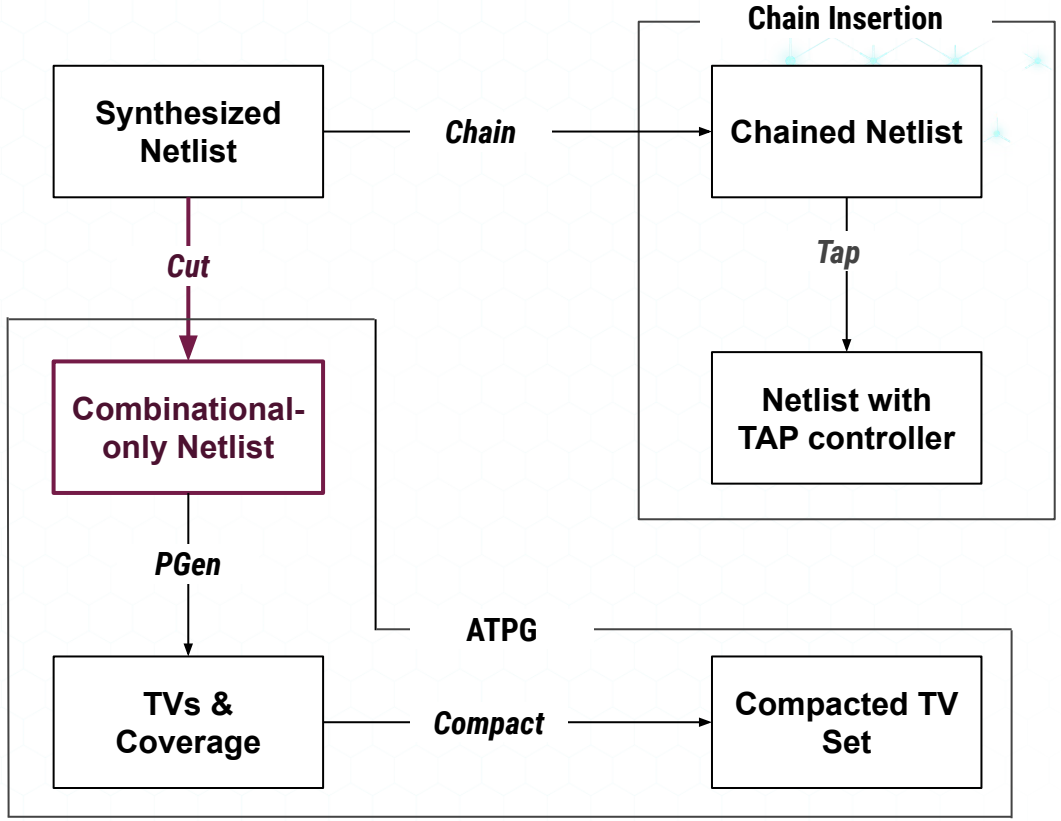
> To fill the gap in open-source DFT solutions by being open-source, supporting standard EDA-formats , and by supporting a complete DFT flow



Fault Flow


Chain Insertion
Synthesized Netlist
Chain
Chained Netlist
Tap
Cut
Netlist with TAP controller
Comb-only Netlist
PGen
Automatic Test Pattern Generation (ATPG)
TVs & Coverage
Compact
Compacted TV Set

Fault Flow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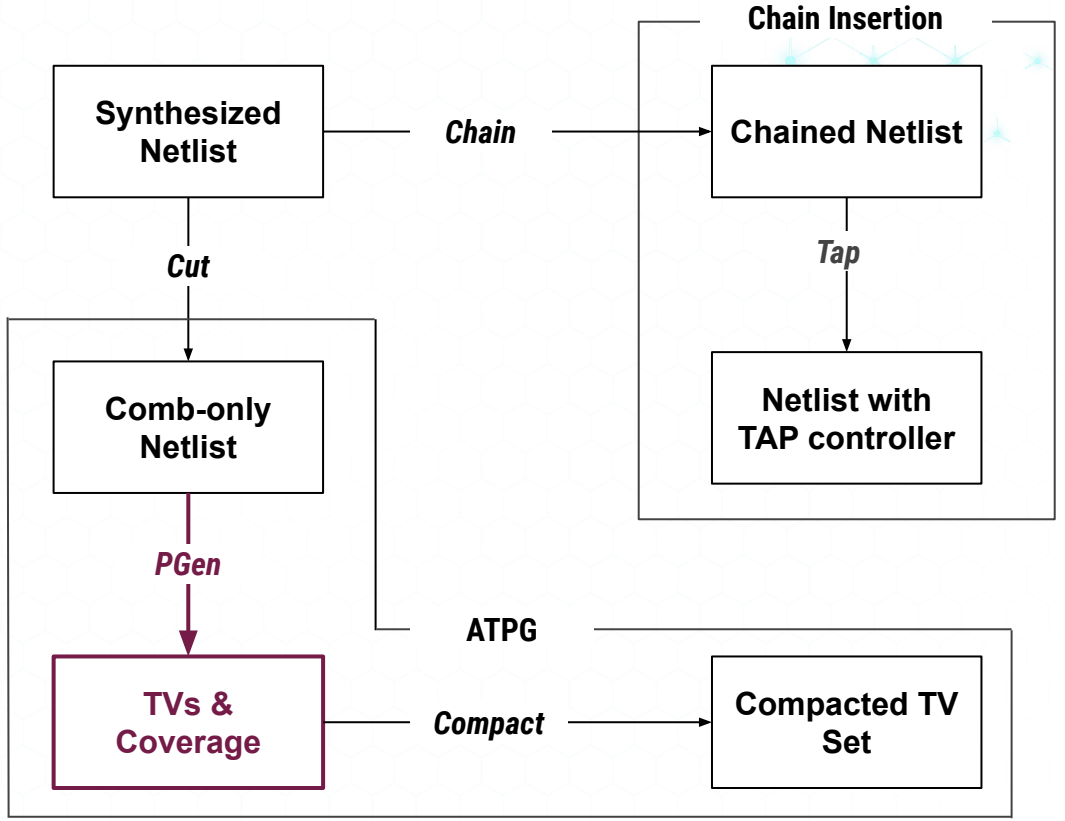
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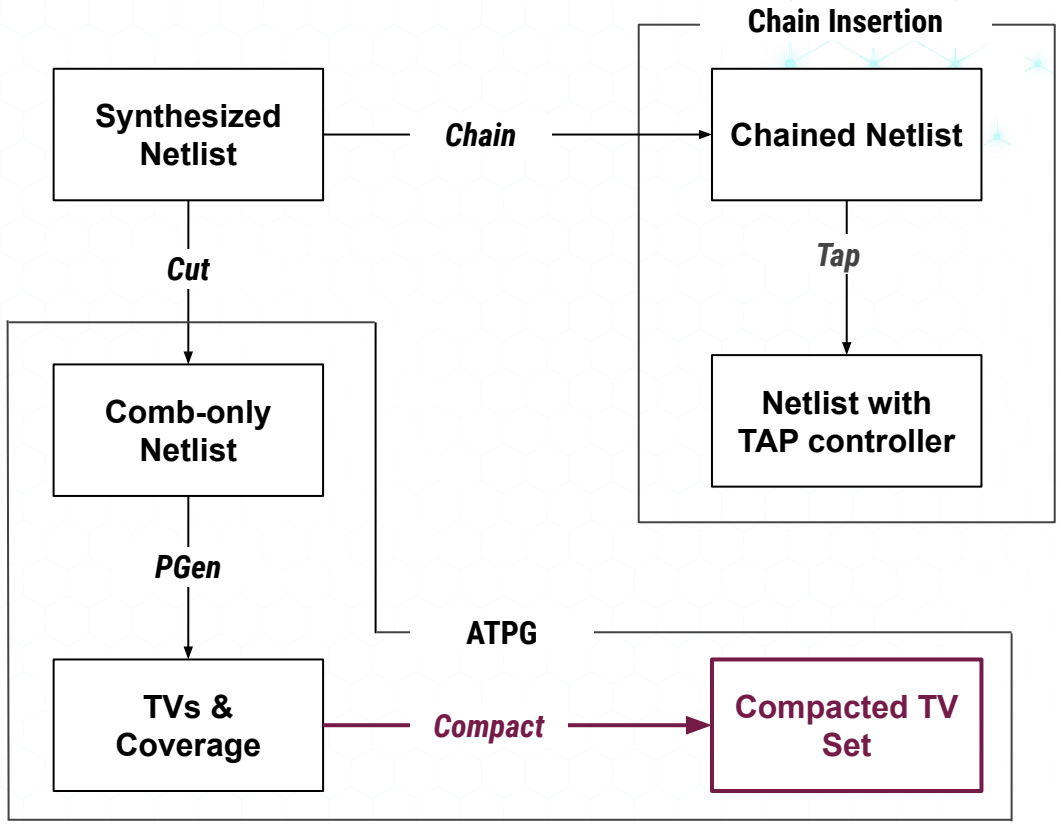
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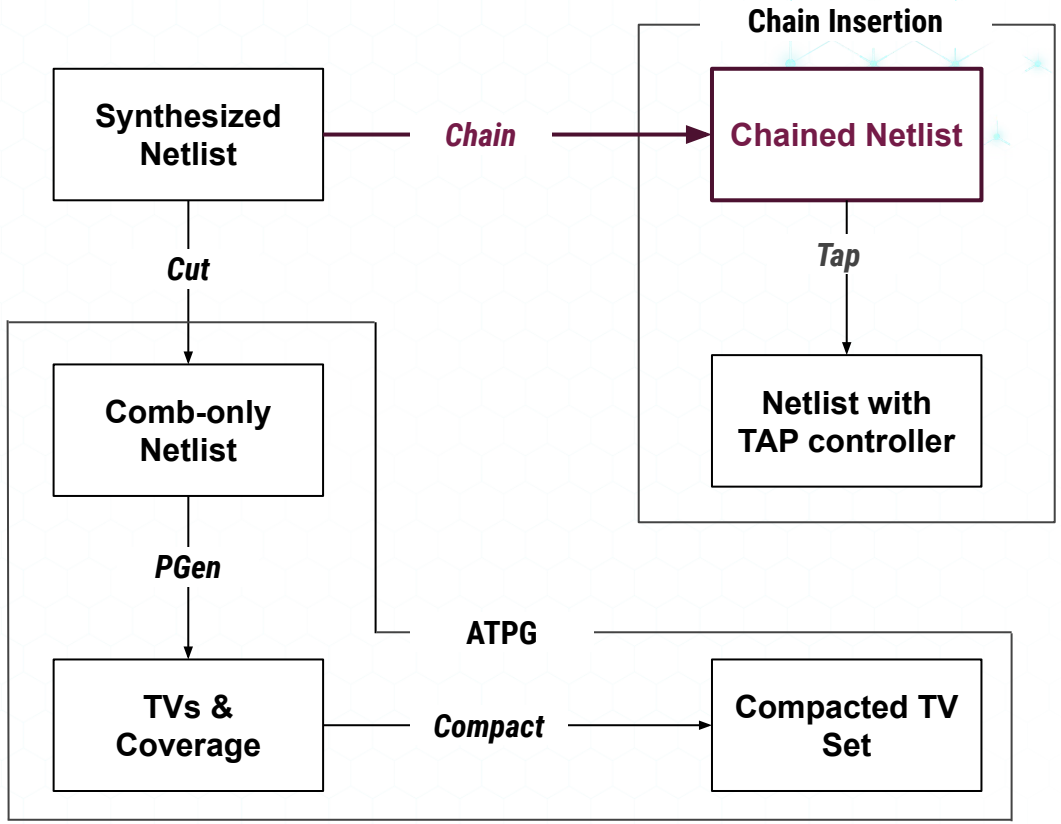
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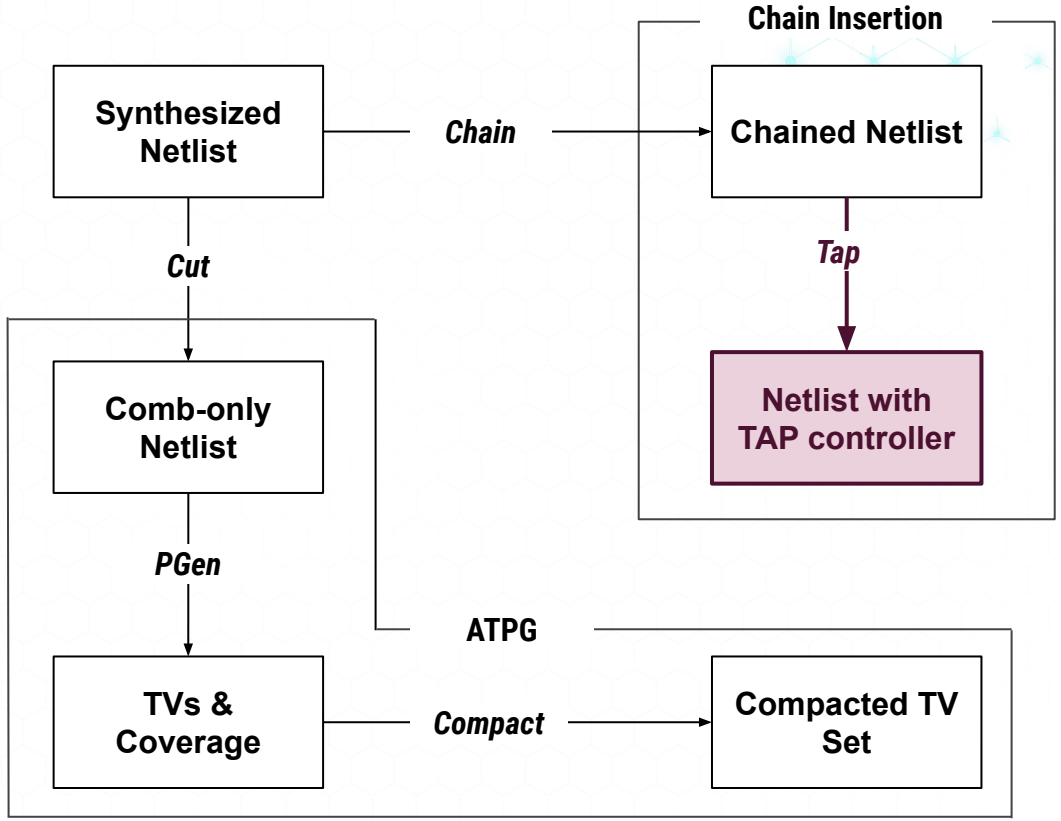
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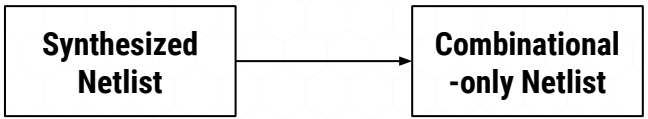
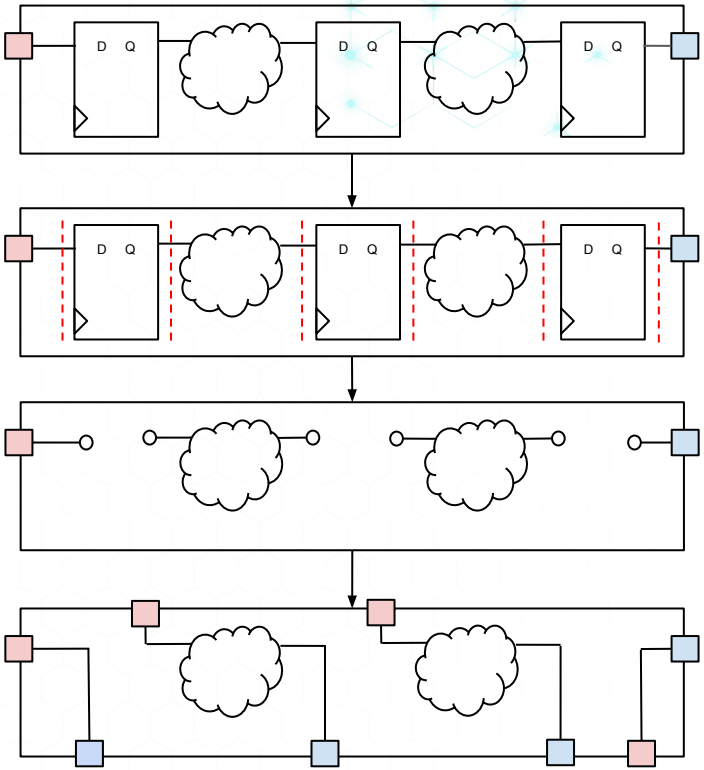
01

Cut

- Converts sequential circuit to a pure combinational one.
- The generated netlist is then used by the ATPG process.

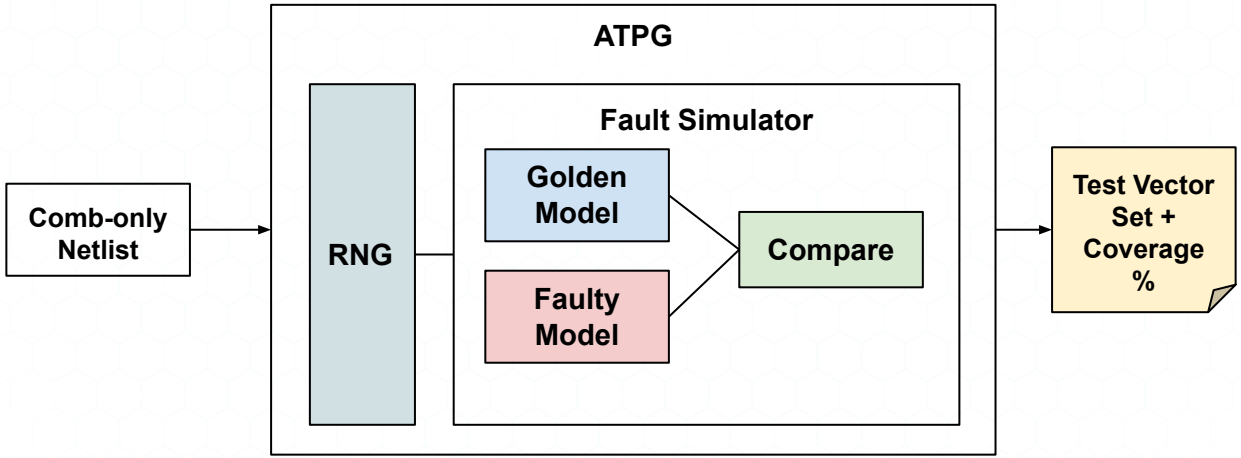




02

PGen (ATPG)

- Test vectors are pseudo-randomly generated.



03

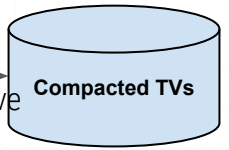
Compact

- Static test vector compaction.
- Reduces the number of TVs without affecting the coverage.

	fs0 (sa0)	fs0 (sa1)	....	fsn (sa0)	fsn (sa1)
TV1	1	0	....	0	1
TV2	0	0	....	0	1
....	...	....	...	...	...
TVn	1	0	...	1	0

Successively remove row with highest #of detectable faults

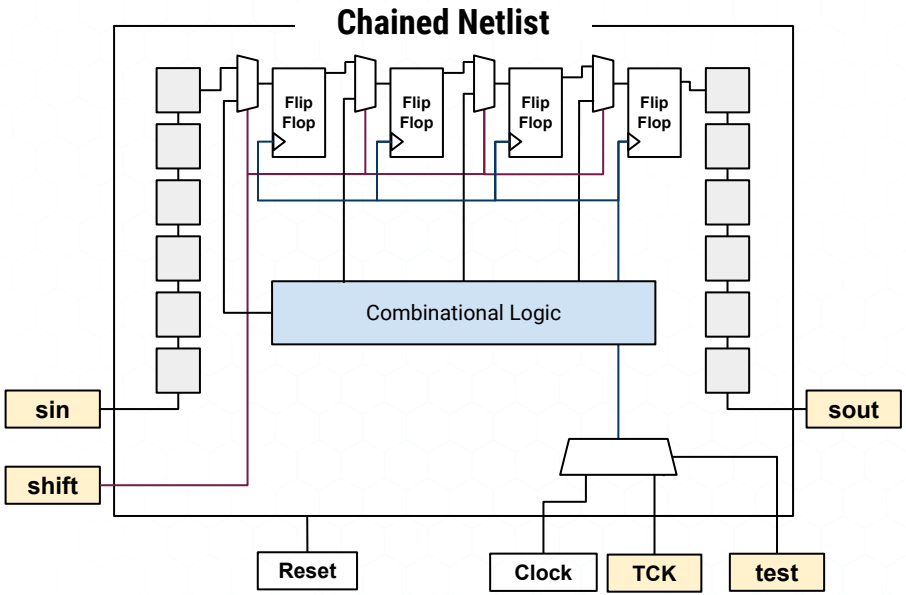
& the detectable faults respective columns

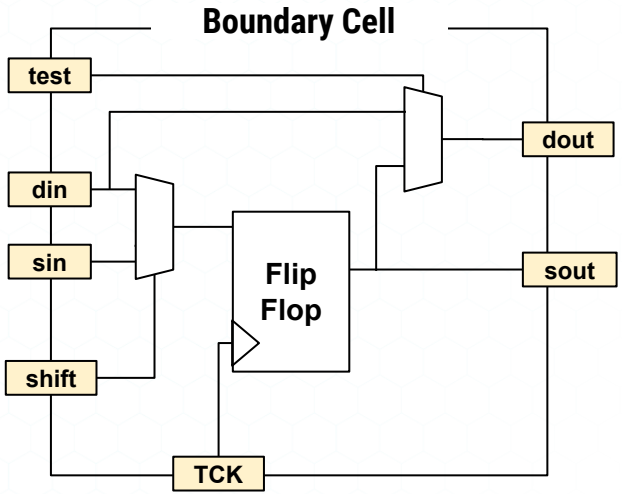


04

Chain

- Automatic scan-chain insertion.

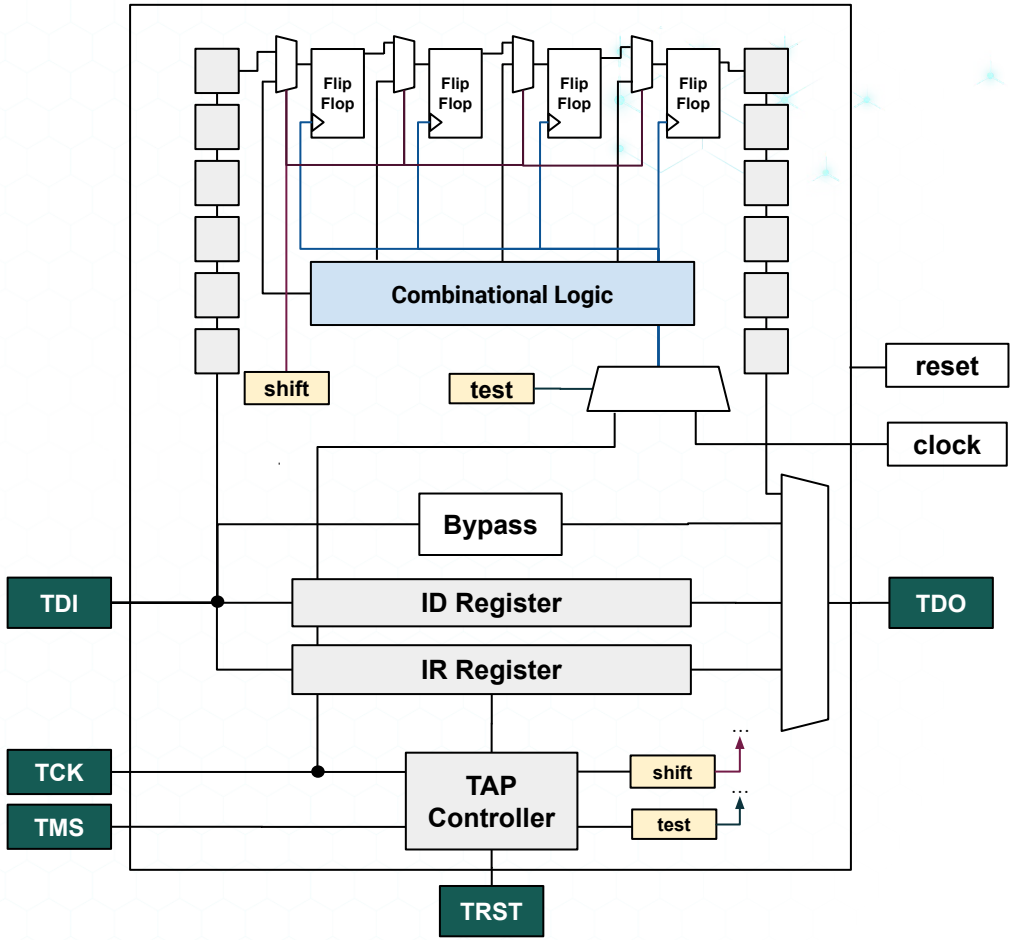




05

Tap

- Stitches JTAG controller to the chained netlist.
- Five Tap Ports:
  - TDI
  - TMS
  - TCK
  - TDO
  - TRST

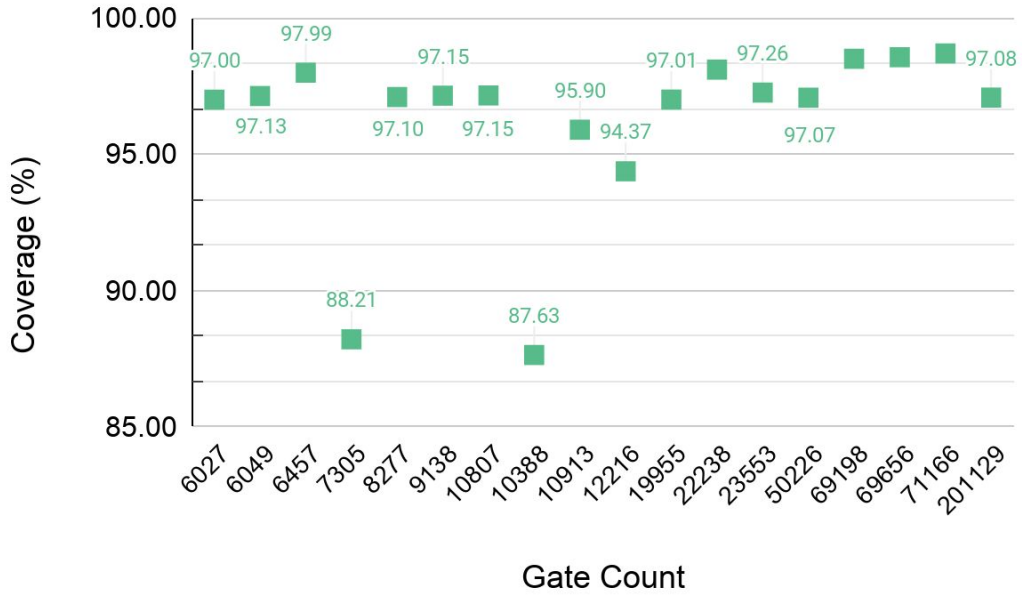


Benchmarking & Performance

Results of Fault's flow.

Coverage vs. Gate Count

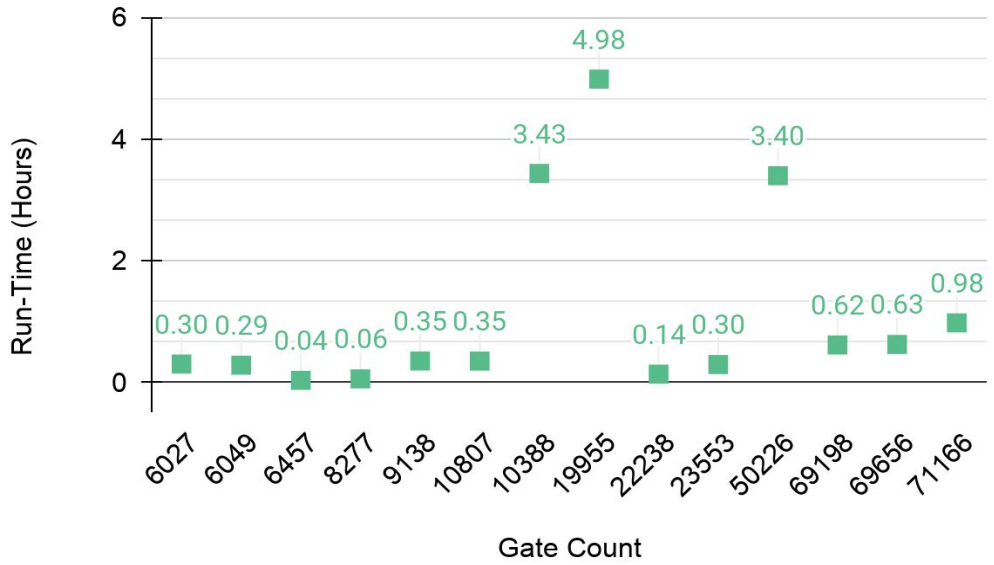
- Average ~ 96%



Gate Count	Coverage (%)
201129	97.08
71166	98.70
69656	98.56
69198	98.50
50226	97.07
23553	97.26
22238	98.10
19955	97.01
12216	94.37
10913	95.90
10388	87.63
10807	97.15
9138	97.15
8277	97.10
7305	88.21
6457	97.99
6049	97.13
6027	97.00

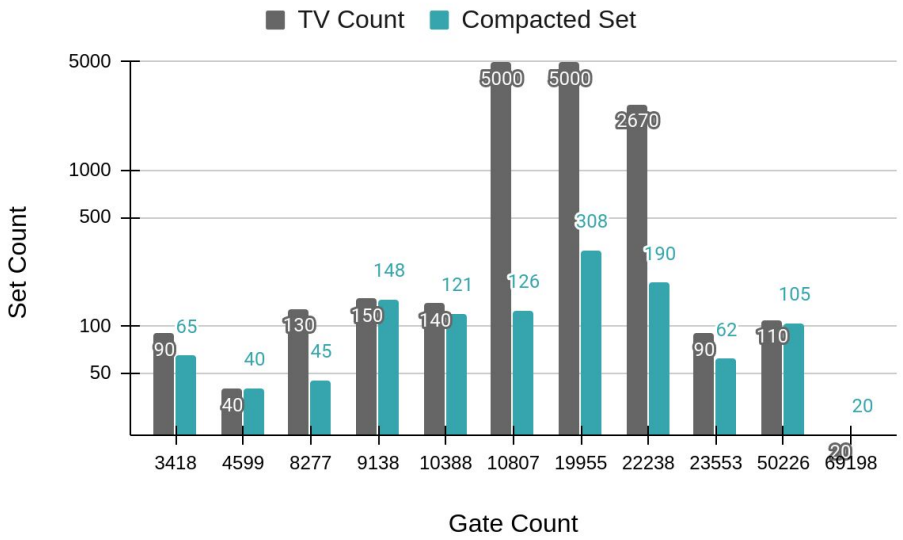
Run-time vs. Gate Count

- Average ~ 1.13 Hours (10 Threads & 32 GB of RAM)



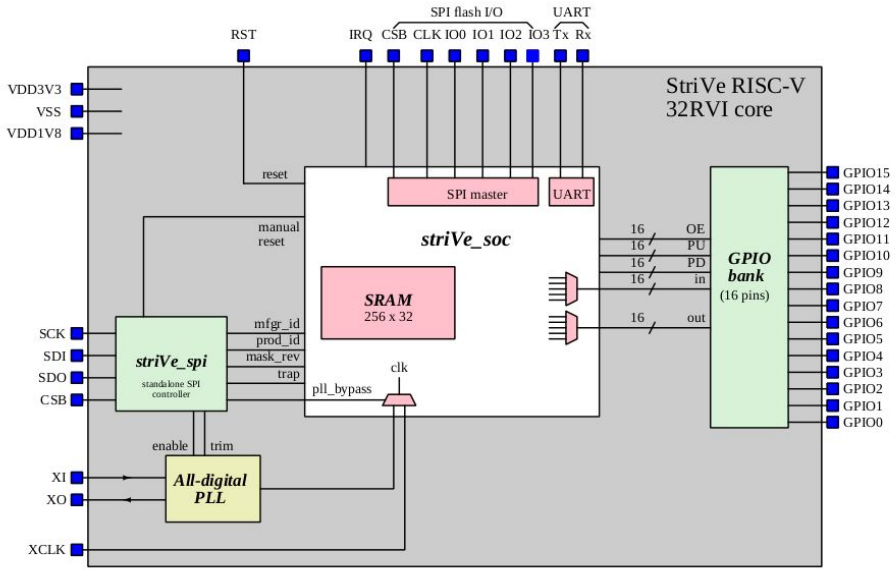
Gate Count	Run-Time (Hrs)
71166	0.98
69656	0.63
69198	0.62
50226	3.40
23553	0.30
22238	0.14
19955	4.98
10388	3.43
10807	0.35
9138	0.35
8277	0.06
6457	0.04
6049	0.29
6027	0.30

Compaction



Gate Count	TV Count	Compacted Set
69198	20	20
50226	110	105
23553	90	62
22238	2670	190
19955	5000	308
10807	5000	126
10388	140	121
9138	150	148
8277	130	45
4599	40	40
3418	90	65

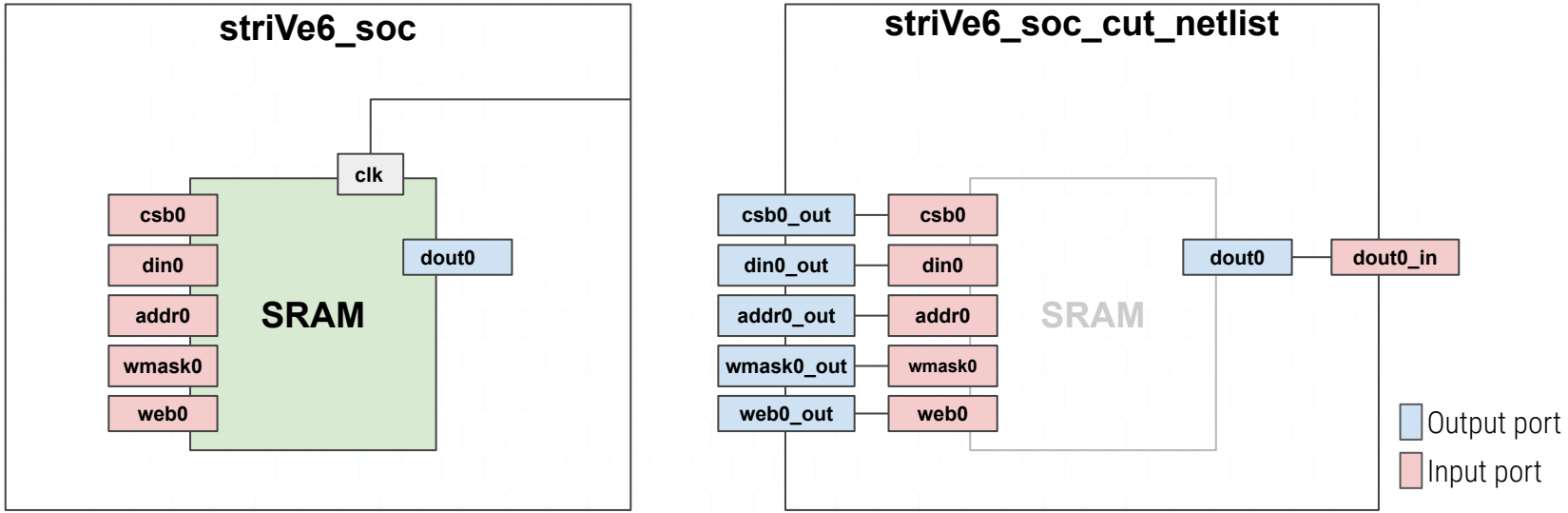
striVe6 Tape-out



striVe6 Cut Netlist

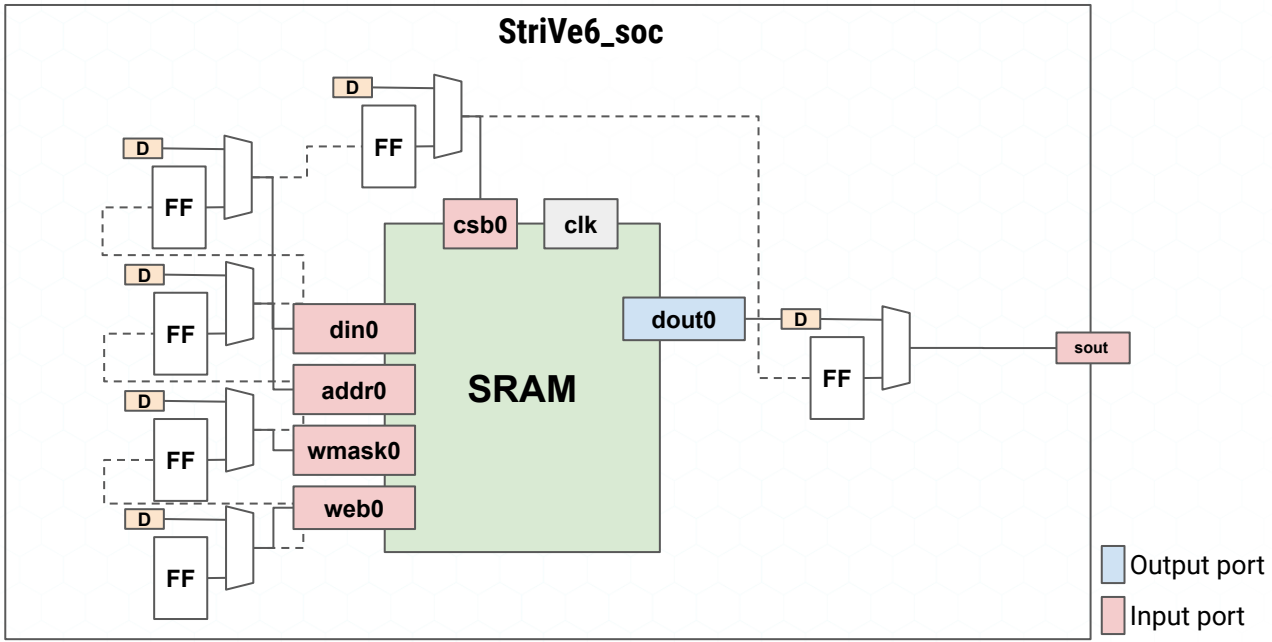
Lessons learned:

- How to support hard non-scannable blocks like the SRAM ?



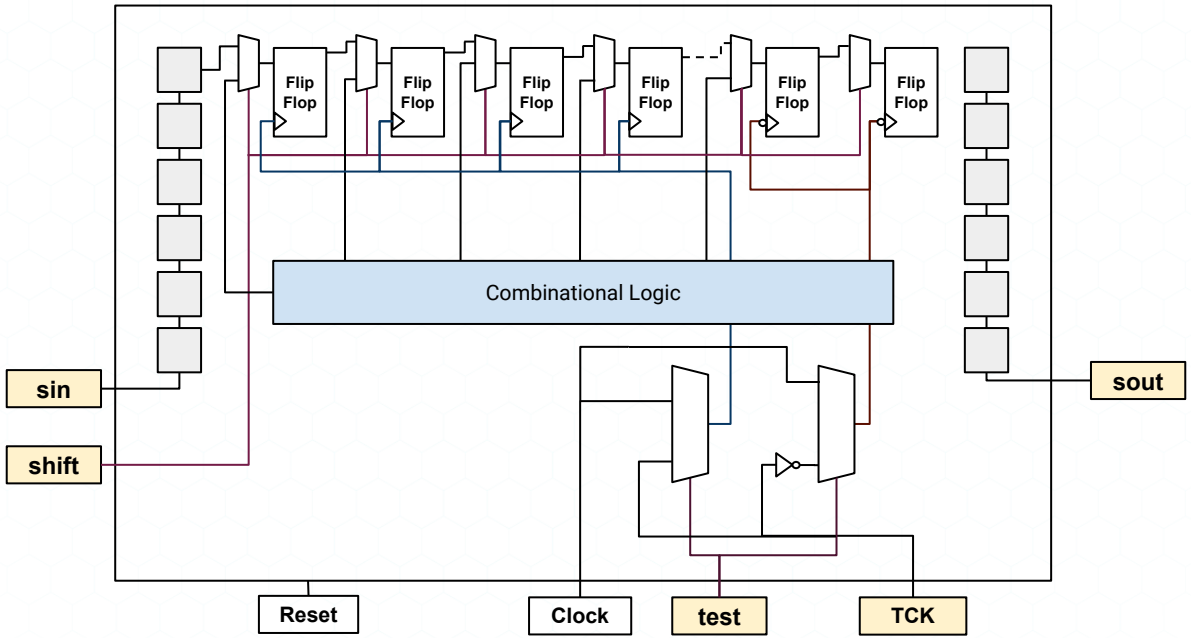
striVe6 Scan Chain

- How to bypass sram while in test mode ?
  - Connecting a scan-cell to each input and output port.



striVe6 Scan Chain

- How to handle flip-flops with different clock-edge sensitivity ?



striVe6 ATPG

- **ATPG process parameters**

Number of threads	10
Ceiling	5000 TVs
Min Coverage	97%

- **Concluded with**

Coverage	90%
Compacted TVs	311 TVs

Conclusion

Fault is the **only complete & practical** open source DFT toolchain that supports standard EDA formats.

Future Work

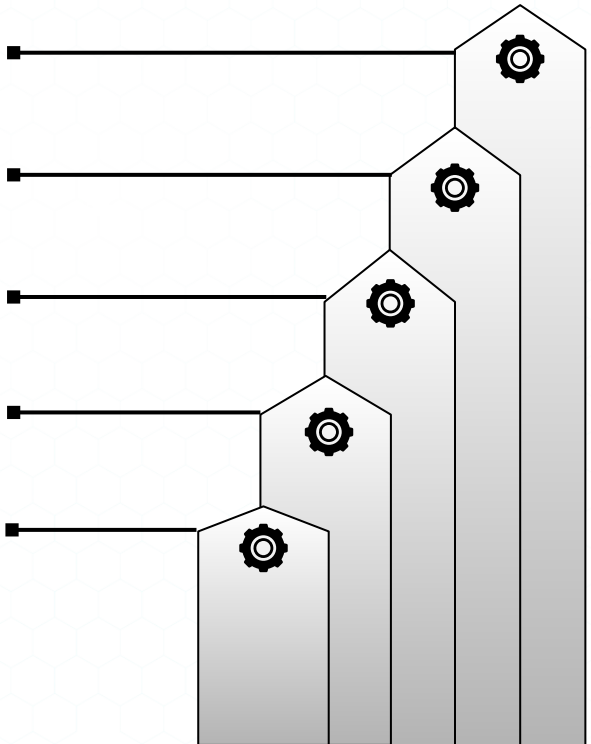
Algorithmic TV generation.

Fault collapsing

BIST support for memory and logic.

Support of other fault models like transition faults.

Use of compiled simulators



Open-Source Acknowledgment

Yosys

RTL Synthesis

Pyverilog

Netlist cutting, scan chain insertion, and JTAG controller stitching

Icarus Verilog

Testbench Simulations

Thanks

Find Us

https://github.com/Cloud-V/Fault