MANAR ABDELATTY

+1(848) 203-1045 ◇ Providence, RI
manar_abdelatty@brown.edu ◇ linkedin.com/in/manar-abdelatty-8025b7141/ ◇ manarabdelaty.github.io.

EDUCATION

PhD in Electrical and Computer Engineering, Brown University — Jan 2022 - Dec 2026
Advisor: Sherief Reda, Co-advisor: Jacob Rosenstein
Expected Graduation Data: 12/31/2026
GPA: 4.0

Masters of Science in Electrical and Computer Engineering, Brown University — Jan 2022 - May 2024
Relevant Coursework: Mixed-Signal Electronic Design, Deep Learning,
Machine Learning and Pattern Recognition, Computer Vision, Design and Analysis of Algorithms.
GPA: 4.0

Bachelor of Science in Computer Engineering, American University in Cairo — 2015 - 2020
Thesis: Fully autonomous navigation kit using LIDAR and odometery sensors. **Github**
Graduated *summa cum laude*, GPA: 3.9

TECHNICAL SKILLS

Programming Languages	C/C++, Python, Swift, TCL
Machine Learning Frameworks	Pytorch, Tensorflow, JAX, Keras
Hardware Design	Verilog, SPICE
EDA Tools	Cadence Genus, Virtuoso, Synopsys DC Compiler, Calibre

WORK EXPERIENCE

Research Assistant at SCALE Lab — Jan 2022 - Present
Brown University — *Providence, RI*

- Conducting research on leveraging large language models for accelerating hardware design workflows.
- Collaborated with interdisciplinary teams on integrating machine learning for data enhancement of microelectronic circuits.

Hardware Technology Intern — Jun 2025 - Aug 2025
Apple — *Cupertino, CA*

- Developed an LLM-assisted library analysis workflow for liberty data and release notes.
- Built a multi-agent framework for Timing ECO recommendations and timing report analysis.

EDA Engineer — Jun 2020 - Jan 2022
Efabless — *San Jose, CA*

- Designed and Taped-out RISC-V system-on-chips (SoCs) on the *Skywater PDK* shuttle programs.
- Took main responsibility of running the physical implementation of the digital blocks of the *Caravel* chip.
- Automated the digital design flow in TCL, as part of the *OpenLane* team.
- Conducted sign-off checks including gate-level simulations, timing analysis, and DRC/LVS checks using Calibre and open-source tools.

Research Assistant — Sep 2019 - Jun 2020
American University in Cairo — *Cairo, Egypt*

- Conducted research in the digital design field and design-for-testing (DFT).
- Co-developed an open-source design-for-testing toolchain, *Fault*, in Swift.

TEACHING EXPERIENCE

Graduate Teaching Assistant — CSCE 432/4301 Embedded Systems Spring 2021
American University in Cairo *Cairo, Egypt*

- Graded assignments and exams and gave feedback on students work.
- Conducted review sessions before the exams and prepared review sheets.

Graduate Teaching Assistant — ECNG 525/5225 Digital Signal Processing Spring 2021
American University in Cairo *Cairo, Egypt*

- Graded homeworks and midterm exams.
- Provided feedback on student's work in the final project.

Graduate Teaching Assistant — CSCE 337/3304 Digital Design II Summer 2020 - Fall 2021
American University in Cairo *Cairo, Egypt*

- Co-designed lab handouts with the instructor.
- Taught bi-weekly lab tutorials on running physical design flows.

AWARDS

- **Best Paper Award**, IEEE International Conference on LLM-Aided Design, Stanford, Summer 2025
- **Design Automation Conference (DAC) Young Fellow**, California, San Francisco, Summer 2022
- **Mohammed Bin Abdulkarim Endowed Undergraduate Award**, Spring 2020 (AUC). This award is given to the highest performing student in STEM fields biannually at the American University in Cairo.
- **Third Place Award at AUC Robotics Conference Research Competition**, Winter 2019 (AUC).
- **Grant Recepient from ITAC ITIDA**, Spring 2019 (AUC). For sponsoring my graduation project on developing a fully autonomous navigation kit using LIDAR and odometry sensors.
- **AT & T Endowed Scholarship Recipient**, Fall 2015 (AUC). Awarded yearly for students majoring in engineering based on their academic merit.

PUBLICATIONS

[6] **M. Abdelatty***, M. Nouh*, J. K. Rosenstein, and S. Reda, **"Pluto: A Benchmark for Evaluating Efficiency of LLM-Generated Hardware Code"** Preprint, Under Review, 2025. (*denotes first co-authors) Paper

[5] **M. Abdelatty**, J. K. Rosenstein, and S. Reda, **"ChipXplore: Natural Language Exploration of Hardware Designs and Libraries"** IEEE International Conference on LLM-Aided Design (LAD), 2025. Paper ***Best Paper Award***

[4] **M. Abdelatty**, J. Ma, and S. Reda, **"MetRex: A Benchmark for Verilog Code Metric Reasoning Using LLMs"**, IEEE Asia and South Pacific Design Automation Conference (ASP-DAC), 2025. Paper

[3] **M. Abdelatty**, J. T. Incandela, K. Hu, P. Joshi, J. W. Larkin, S. Reda, and J. K. Rosenstein, **"Electrical Capacitance Tomography of Cell Cultures on a CMOS Microelectrode Array,"** IEEE Transactions on Biomedical Circuits and Systems. (TBioCAS), 2024. Paper

[2] **M. Abdelatty**, J. T. Incandela, K. Hu, J. W. Larkin, S. Reda, and J. K. Rosenstein, **"Microscale 3-D Capacitance Tomography with a CMOS Sensor Array"** in Proceedings of IEEE Biomedical Circuits and Systems (BioCAS), 2023. Paper

[1] **M. Abdelatty**, M. Gaber, and M. Shalan, **"Fault: Open Source EDA's Missing DFT Toolchain"** IEEE Design & Test, vol. 38, no. 2, pp. 55-62, Apr. 2021. Paper

[0] M. Gaber, **M. Abdelatty**, and M. Shalan, **"Fault, an Open Source DFT Toolchain"** in Workshop on Open-Source EDA Technology (WOSET), 2019. Paper